

Digital Logic Design

LAB – 03

Universal Logic Gates

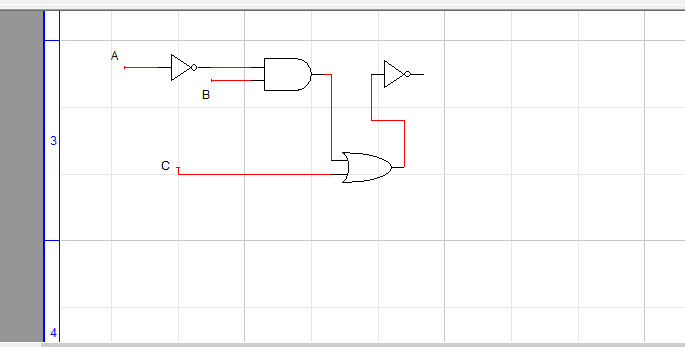
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* Student name: Muhammad Bilal

**Lab Task#1:**

((A.B + C.D)’ +B’)’.C

**Lab Task#2:**

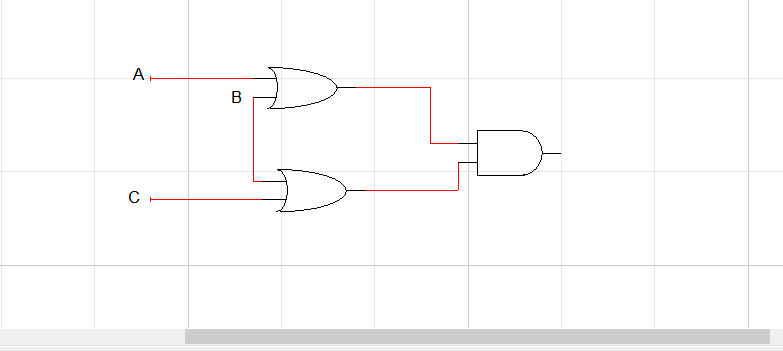
(A’B + C)’



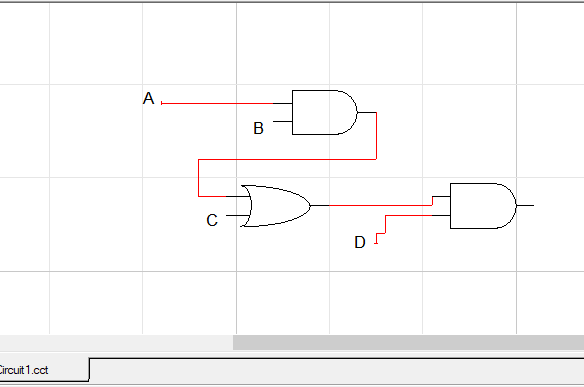
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | y |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Lab Task#3:**

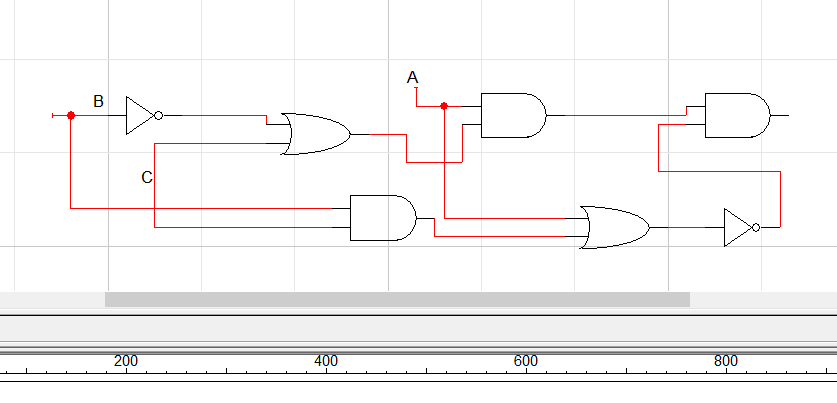
1.



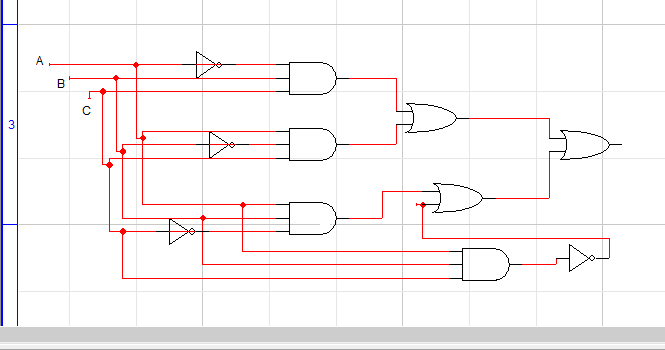
2.



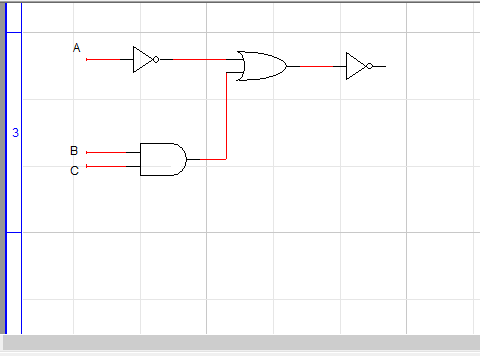
3.



4.



5.



**Lab Task#4:**

